

REMARK

Applicant respectfully requests reconsideration of this application as amended.
All existing claims have been cancelled, and new claims 21-46 have been added.
Therefore, claims 21-46 are present for examination.

Specification

As indicated in the Office Action, the title of the invention, as provided on page 1, line 1 of the application, was incorrect. The correct title, as shown on the title page and the declaration, is "Kicker for Non-Volatile Memory Drain Bias". The specification has been amended to correct this error.

In addition, it is noted that the filing receipt also contains the incorrect title. A request to correct the filing receipt is being filed.

35 U.S.C. §102 Rejection

The Examiner rejected claims 1-20 under 35 U.S.C. 102(e), as being anticipated by U.S. Patent No. 6,097,633 of La Placa ("La Placa"). Claims 1-20 have been cancelled herein, replaced by claims 21-⁴⁵~~46~~.

It is submitted that La Placa contains a different method for addressing voltages and node relationships in non-volatile memory devices and for this reason does not anticipate the provisions of the claims herein.

Claim 21, as added herein, provides for the following:

21. A method comprising:

providing an electrical pulse to a first drain bias circuit for a first
non-volatile memory cell;

in response to the electrical pulse:

pulling a voltage of the first drain bias towards a voltage
potential of a supply source; and
shorting a sense node for the non-volatile memory cell to a
reference node.

Claim 21 differs from La Placa in numerous ways. One difference is that La Placa does not provide for shorting the sense node for a non-volatile memory cell to a reference node. In the present application, this is shown in the specification in Figure 6, where element 680 is coupled between a sense node and a reference node. In La Placa, there is no such coupling discussed or shown in the figures. For example, Figure 2 of La Placa shows no connections between the data and reference sides of the circuit other than the final connections to the differential amplifier, element 2.

Another difference is that La Placa does not include providing an electrical pulse in its relevant operations. Instead, La Place provides only an enable signal for the differential amplifier described. As long as the enable signal is low, thus when the differential amplifier is not enabled, the nodes coupled to the differential amplifier remain at the power supply voltage. (La Placa, col. 3, lines 11-14) Operating nodes at a voltage whenever a differential amplifier is not enabled is not equivalent to applying a pulse to a drain bias circuit.

For at least these reasons, La Placa does not anticipate claim 21. It is submitted that the arguments presented herein are also applicable to independent claims 30 and 39 and thus such claims are not anticipated by La Placa. The remaining claims are dependent claims and, while having other distinguishing elements that are not anticipated by La Placa, are allowable because they are dependent on the allowable base claims.

CONCLUSION

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Charge our Deposit Account

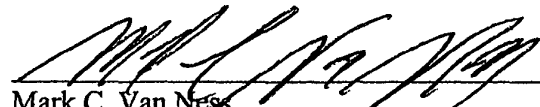
Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date:

6/24/02


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AMENDMENTS -- MARKED VERSION

Presented below are the amendments with markings to indicate changes made.

In the Specification:

Please delete the heading at page 2, line 1, and substitute the following:

--KICKER FOR NON-VOLATILE MEMORY DRAIN BIAS--

In the Claims:

Please delete claims 1-20 without prejudice.

Please amend the claims as follows:

1-20. [cancelled]

Please add the following new claims

21. (New) --A method comprising:

providing an electrical pulse to a first drain bias circuit for a first non-volatile
memory cell;

in response to the electrical pulse:

pulling a voltage of the first drain bias towards a voltage potential of a
supply source; and

shorting a sense node for the non-volatile memory cell to a reference
node.--

22. (New) --The method of claim 21, wherein said first non-volatile memory cell is a
flash memory cell.--

23. (New) --The method of claim 22, wherein pulling a voltage of the first drain bias towards a voltage potential of a supply voltage comprises enabling a first kicker device coupled to the drain bias for the first non-volatile memory cell.--
24. (New) --The method of claim 23, wherein said high performance transistor is a P-channel semiconductor device.--
25. (New) --The method of claim 23, wherein shorting the sense node to the reference node comprises enabling a semiconductor device coupled between the sense node and the reference node.--
26. (New) --The method of claim 25, wherein the semiconductor device comprises an s' device.--
27. (New) --The method of claim 25, wherein the electrical pulse is provided prior to sensing the contents of said first non-volatile memory cell.--
28. (New) --The method of claim 25, wherein the first non-volatile memory cell is included in a data array, and further comprising enabling a second kicker device for a second drain bias circuit for a memory cell included in a reference array, the voltage of the first drain bias circuit and a voltage of the second drain bias circuit being pulled towards the same voltage potential.--
29. (New) --The method of claim 25, wherein the first drain bias comprises a cascode amplifier.--
30. (New) --An apparatus comprising:

a kicker device, a first terminal of the kicker device being coupled to a voltage from a supply voltage and a second terminal of the kicker device being coupled to a drain bias circuit for a memory cell of a non-volatile memory device;

a semiconductor device, a first terminal of the semiconductor device being coupled to a sense node of the non-volatile memory cell and a second terminal of the semiconductor device being coupled to a reference node; and

the kicker device and the semiconductor device being enabled by an enable signal pulse.--

32. (New) --The apparatus of claim 31, wherein the non-volatile memory device is a flash memory device.--
33. (New) --The apparatus of claim 32, wherein the enable pulse is received prior to sensing the contents of the non-volatile memory cell.--
34. (New) --The apparatus of claim 33, wherein the kicker device is a high performance transistor.--
35. (New) --The apparatus of claim 34, wherein the high performance transistor is a P-channel semiconductor device.--
36. (New) --The apparatus of claim 33, wherein the kicker pulls the voltage of a node towards the voltage potential of a supply source.--

37. (New) --The apparatus of claim 33, wherein enabling the semiconductor device comprises equalizing the voltage potential of the sense node with the voltage potential of the reference node during bit charging.--
38. (New) --The apparatus of claim 33, wherein the non-volatile memory drain bias circuit comprises a cascode amplifier.--
39. (New) --A non-volatile memory device, comprising:
an array of memory cells;
an array of reference cells;
a first drain bias circuit for a first memory cell in the array of memory cells;
a kicker device, a first terminal of the kicker device being coupled to a voltage from a supply voltage and a second terminal of the kicker device being coupled to the first drain bias circuit;
a semiconductor device, a first terminal of the semiconductor device being coupled to a sense node of the first memory cell and a second terminal of the semiconductor device being coupled to a reference node of a first reference cell in the array of reference cells; and
the kicker device and the semiconductor device being enabled by an enable signal pulse.--
40. (New) --The non-volatile memory device of claim 39, wherein the non-volatile memory device is a flash memory device.--
41. (New) --The non-volatile memory device of claim 40, wherein the enable pulse is received prior to sensing the contents of the first memory cell.--

42. (New) --The non-volatile memory device of claim 41, wherein the kicker device is a high performance transistor.--
43. (New) --The non-volatile memory device of claim 42, wherein the high performance transistor is a P-channel semiconductor device.--
44. (New) --The non-volatile memory device of claim 43, wherein the kicker pulls the voltage of a node towards the voltage potential of a supply source.--
45. (New) --The non-volatile memory device of claim 41, wherein enabling the semiconductor device comprises equalizing the voltage potential of the sense node with the voltage potential of the reference node during bit charging.--
46. (New) --The non-volatile memory device of claim 33, wherein the first drain bias circuit comprises a cascode amplifier.--